

Appendix A

Following is a pin definition file for the master FPGA of a board of the present invention.

5
//
// HEADER FILE FOR MASTER FPGA
//
//
10
#ifndef _KOMPRESSOR_MASTER_HEADER
#define _KOMPRESSOR_MASTER_HEADER
15 #warning Compiling design for the Master FPGA

// Set part and family numbers
20 set part = "XV2000e-6-FG680";
set family = Xilinx4000E; // check there definitions

//
// Clocks
25 //

// CLKA A20
// CLKB D21
// MCLK AU22

09772534.012901.T062T0.452260

// VCLK AW19

// Only one clock is currently supported (HC2.1)

set clock = external_divide "A20" 2;

5

#define CLOCK_RATE 25000000 // 50MHz clock / 2

#define VGA // necessary for VGA driver

10

////////////////////////////////////

// Master Slave definition Pin

////////////////////////////////////

15

macro expr MS_define = { data = {"C9"}};

////////////////////////////////////

// Local SRAM definitions

20

////////////////////////////////////

////////////////////////////////////

// Local SRAM BANK 0

//

25

// Though this bank is defined to be 32bits wide.

// it is possible to perform 8bit writes if required.

////////////////////////////////////

FOR TEST - 01290

```
macro expr DA_pins = {"W1", "AB4", "AB3", "W2", "AB2", "V1", "AA4", "V2",  
"AA3", "U1",  
    "W3", "U2", "W4", "T1", "V3", "T2", "V4", "V5", "U3", "R2", "U4",  
    "P1", "U5", "P2", "T3", "N1", "N2", "T4", "M1", "R3", "M2", "R4"};
```

5

```
macro expr AA_pins = {"L1", "L2", "N3", "K1", "N4", "K2", "M3", "J1",  
    "L3", "J2", "L4", "H1", "K3", "H2", "K4", "G1", "G2", "J3"};
```

```
macro expr CA_pins = {data = {"F1", "J4", "F2", "H3", "E1", "H4", "E2"}};
```

10

```
macro expr sram_local_bank0_spec =  
{  
    offchip = 1,  
    wegate = 1,    // we are using a divide 2 clock  
    data = DA_pins,  
    addr = AA_pins,  
    cs  = {"E2", "F1", "J4", "F2", "H3"},  
    we  = {"H4"},  
    oe  = {"E1"}  
};
```

20

```
25  ///////////////////////////////////  
    // Local SRAM Bank 1  
    ///////////////////////////////////
```

T062T0"hes2460

```
macro expr DB_pins = {"AT3", "AP3", "AR3", "AT2", "AP4", "AR2", "AT1", "AN4",  
"AR1",  
"AN3", "AP2", "AN2", "AP1", "AM4", "AN1", "AM3", "AL4", "AM2",  
"AL3",  
5 "AM1", "AL2", "AL1", "AK4", "AK2", "AK3", "AK1", "AJ4", "AJ1",  
"AJ3",  
"AH2", "AJ2", "AH3"};
```

```
macro expr AB_pins = {"AG1", "AG4", "AF2", "AG3", "AF1", "AF4", "AF3", "AE2",  
10 "AE4",  
"AE1", "AE3", "AD2", "AD4", "AD1", "AC1", "AB1", "AC5", "AA2"};
```

```
macro expr CB_pins = {data = {"AC4", "AA1", "AC3", "Y1", "AC2", "Y2", "AB5"}};
```

```
15 macro expr sram_local_bank1_spec =  
{  
offchip = 1,  
wegate = 1,  
20 data = DB_pins,  
addr = AB_pins,  
cs = {"AB5", "AC4", "AA1", "AC3", "Y1"},  
we = {"Y2"},  
oe = {"AC2"}  
25 };
```

```
////////////////////////////////
```

007524-01901
T062T0-HE52460

// Shared SRAM definitions

////////////////////////////////

////////////////////////////////

5 // Shared SRAM BANK 0

//

// Though this bank is defined to be 32bits wide.

// it is possible to perform 8bit writes if required.

////////////////////////////////

10

macro expr SHAREDGRAM0A_pins = { "R37", "M39", "R36", "M38", "P37", "L39",
"P36", "N37", "L38", "N36", "K39", "M37", "K38",
"L37", "J39", "L36", "J38", "K37"};

15

macro expr SHAREDGRAM0D_pins = { "AA39", "AB35", "Y38", "AB36", "Y39",
"AB37",
"AA36", "W39", "AA37", "W38", "W37", "V39", "W36",
"U39", "V38", "U38", "V37", "T39", "V36", "T38",
"V35", "R39", "U37", "U36", "R38", "U35", "P39",
"T37", "P38", "T36", "N39", "N38"};

20

macro expr sram_shared_bank0_request_pin = { data = { "A17" } };

macro expr sram_shared_bank0_grant_pin = { data = { "B17" } };

25

macro expr sram_shared_bank0_spec =
{
offchip = 1,
wegate = 1,
data = SHAREDGRAM0D_pins,

```
addr = SHAREDGRAM0A_pins,
cs  = { "J36", "H39", "K36", "H38", "J37"},
we  = { "G38" },
oe  = { "G39" }
5   };

10  //////////////////////////////////
    // Shared RAM bank1
    //////////////////////////////////

15  macro expr SHAREDGRAM1A_pins = { "AH39", "AG38", "AG36", "AG39", "AG37",
    "AF39", "AF36",
        "AE38", "AF37", "AF38", "AE39", "AE36", "AD38", "AE37",
        "AD39", "AD36", "AC38", "AC39"};

20  macro expr SHAREDGRAM1D_pins = { "AR37", "AR39", "AR36", "AT38", "AR38",
    "AP36", "AT39",
        "AP37", "AP38", "AP39", "AN36", "AN38", "AN37", "AN39",
        "AM36", "AM38", "AM37", "AL36", "AM39", "AL37", "AL38",
        "AK36", "AL39", "AK37", "AK38", "AJ36", "AK39", "AJ37",
25  "AJ38", "AH37", "AJ39", "AH38"};

macro expr sram_shared_bank1_request_pin = { data = { "D18" } };
macro expr sram_shared_bank1_grant_pin  = { data = { "E18" } };
```

macro expr sram_shared_bank1_spec =

{

offchip = 1,

5 wegate = 1,

data = SHAREDGRAM1D_pins,

addr = SHAREDGRAM1A_pins,

cs = { "AC37","AD37", "AB38", "AC35", "AB39" },

we = { "AA38" },

10 oe = { "AC36" }

};

15 //

// ARM Interfacing Pins

//

macro expr ARMA_pins = {data = { "A33", "C31", "B32", "B31", "A32", "D30",

20 "A31", "C30", "B30", "D29"}};

macro expr ARMD_pins = {data = { "F39", "H37", "F38", "H36", "E39", "G37",

"E38",

"G36", "D39", "D38", "F36", "D37", "E37", "C38",

25 "B37", "F37", "D35", "B36", "C35", "A36", "D34",

"B35", "C34", "A35", "D33", "B34", "C33", "A34",

"B33", "D32", "C32", "D31"}};

```
macro expr ARMGPIO_pins = {data = { "B9", "D10", "A9", "C10", "B10", "D11",  
"A10",  
"C11", "B11", "C12", "A11"}}};
```

5

```
macro expr ARM_GPIO0_Pin = { data = { "A11"}}};  
macro expr ARM_GPIO1_Pin = { data = { "C12"}}};
```

```
10 macro expr ARMnWE_pin = { data={"A30"}}; // input  
macro expr ARMnOE_pin = { data={"C29"}}; //input  
macro expr ARMnCS4_pin = { data={"A29"}}; // input  
macro expr ARMnCS5_pin = { data={"B29"}}; // input  
macro expr ARMRDY_pin = { data={"B28"}}; //ouput
```

15

```
////////////////////////////////////  
// Flash Memory interface - may not be able to use definiton of Flash as a RAM if  
// FPGA to FPGA configuration is required
```

20

```
////////////////////////////////////
```

```
macro expr FA_pins = { "D23", "A22", "E23", "B22", "B24", "A23", "C24", "B23",  
"A24", "D24", "A25", "C25", "B25", "D25", "A26", "C26",  
"D26", "B26", "C27", "A27", "D27", "B27", "C28", "A28"};
```

25

```
macro expr FD_pins = {"AR4", "AH1", "AG2", "AD3", "R1", "P3", "P4", "C2"}; //  
also to CPLD
```

TOGETHER-012501


```
macro expr FDH_pins = {"B19", "C21", "D22", "B20", "E22", "A21", "C23", "B21"};
```

```
// high byte of the RAM
```

```
macro expr FC_pins = {"C18", "B18", "D19", "A18", "C19"}; // control pins | |oe|
```

```
5 |we|cs
```

```
macro expr flash_addr_spec =
```

```
10 {  
    offchip = 1,  
    data = {},  
    addr = FA_pins,  
    cs = {},  
15    we = {},  
    oe = {}  
};
```

```
macro expr flash_data_spec =
```

```
20 {  
    offchip = 1,  
    data = FD_pins,  
    addr = {},  
    cs = {"C19"},  
25    we = {"A18"},  
    oe = {"B18"}  
};
```

```
macro expr flash_cs_pin = { data = {"C19"}};
```

T052T0"4E52460

```
macro expr flash_oe_pin = { data = {"B18"}};
```

```
macro expr flash_we_pin = { data = {"A18"}};
```

```
macro expr flash_sts_pin = {data = {"D19"}}; // status
```

```
5 macro expr flash_nByte_pin = {data = {"C18"}}; // x8 / x16 selector
```

```
10 //////////////////////////////////////////////////
```

```
// Parallel Port interface
```

```
////////////////////////////////////
```

```
macro expr PP_pins = {data = { "C5", "A4", "D6", "B5", "C6",  
15 "A5", "D7", "B6", "C7", "A6",  
"D8", "B7", "C8", "A7", "D9",  
"B8", "A8"}};
```

```
20 // ppo lines 12 11 10 9 8 6 4 2// pins 2 - 9 on the interface
```

```
macro expr pp_data_pins = {data = { "C6", "A5", "D7", "B6",  
"C7", "D8", "C8", "D9"}};
```

```
25 // Status Port - write to host
```

```
macro expr nAck_pin = { data = { "B5"}}; // ppo 13
```

```
macro expr busy_pin = { data = { "D6"}}; // ppo 14
```

```
macro expr pe_pin = { data = { "A4"}}; // ppo 15
```

```
macro expr select_pin = { data = { "C5"}}; // ppo 16
```

09372534-012901
F062T0-4ES2Z60

```
macro expr nError_pin = { data = { "A7"}};    // ppo 3
macro expr status_port_pins = { data = { "D6", "B5", "A4", "C5", "A7"}};
```

```
5 // Control Port - read from host
macro expr nAutoFeed_pin = { data = { "B8"}};    // ppo 1
macro expr init_pin = { data = { "B7"}};    // ppo 5
macro expr nSelect_in_pin = { data = { "A6"}};    // ppo 7
macro expr nStrobe_pin = { data = { "A8"}};    // ppo 0
```

10

```
//nSelectin, init, nautofeed, strobe,
macro expr control_port_pins = { data = { "A6", "B7", "B8", "A8"}};
```

15

```
////////////////////////////////////
// LEDs - maybe declare subsets and allocate each FPGA some
////////////////////////////////////
```

```
20 macro expr LED_pins = {data = { "AU27", "AW28", "AT26", "AV27",
    "AU26", "AW27", "AV26", "AT25"}};
```

25

```
////////////////////////////////////
// ATA Interface
////////////////////////////////////

macro expr ATA_pins = {data = { "AW12", "AU14", "AV12", "AT14", "AU13",
    "AW11", "AT13", "AV11", "AU12", "AW10", "AU11",
```

FORGET THE 452450

```
"AV10", "AT11", "AW9", "AU10", "AV9", "AT10", "AW8",  
"AU9", "AV8", "AW7", "AT9", "AV7", "AU8", "AW6", "AT8",  
"AV6", "AU7", "AW5", "AT7", "AW4", "AU6", "AV4"}}};
```

5

```
////////////////////////////////////  
// Expansion Bus (32 bits)  
////////////////////////////////////
```

10

```
macro expr E_pins = {data = {"AU23", "AW21", "AV23", "AR22", "AV20",  
    "AW20", "AV19", "AU21", "AW18", "AU19",  
    "AV18", "AT19", "AW17", "AU18", "AV17",  
    "AT18", "AW16", "AR18", "AV16", "AU17",  
    "AT17", "AW15", "AR17", "AV15", "AU16",  
    "AW14", "AT16", "AV14", "AW13", "AU15",  
    "AV13", "AT15"}}};
```

15

20

```
////////////////////////////////////  
// Serial H Bus  
////////////////////////////////////  
macro expr SERIALH_pins = {data = {"G3", "G4", "D2", "F3", "D3", "F4", "D1"}}};
```

25

```
////////////////////////////////////  
// SelectLink Bus - Directly connects the 2 FPGAs
```

T062T04E52460

```
macro expr SL_pins = {data = { "AT34", "AU36", "AU34", "AV36", "AT33",  
    "AW36", "AU33", "AV35", "AT32", "AW35",  
    "AU32", "AV34", "AV32", "AW34", "AT31",  
    "AU31", "AV33", "AT30", "AW33", "AU30",  
    "AW32", "AT29", "AV31", "AU29", "AW31",  
    "AV29", "AV30", "AU28", "AW30", "AT27",  
    "AW29", "AV28"}}};
```

```
//VGA interface
```

```
macro expr vga_vsync_pin = { data = { "AU25" } };
macro expr vga_hsync_pin = { data = { "AW26" } };
macro expr vga_data_pins = { data = { "AV25", "AT24", "AW25", "AU24", "AW24",
"AW23", "AV24", "AV22", "AR23", "AW22", "AT23", "AV21" } };

```

```
macro expr vsync_pin = { "AU25" };
```

```
macro expr hsync_pin = { "AW26" };
```

```
macro expr video_spec = { data = { "AV25", "AT24", "AW25", "AU24",  
    "AW24", "AW23", "AV24", "AV22",  
    "AR23", "AW22", "AT23", "AV21"}}};
```

```
//////////////////////////////////
// CPLD interface pins
5  //////////////////////////////////

macro expr BUSMaster_pin = { data = { "C17" } }; //P12
macro expr FPcom_pins = { data = { "B16", "E17", "A15" } };

10

//////////////////////////////////
// Serial Port pins
//////////////////////////////////

15
macro expr rs232_txd_pin = { data = { "AT6" } };
macro expr rs232_rxd_pin = { data = { "AU4" } };
macro expr rs232_rts_pin = { data = { "AV5" } };
macro expr rs232_cts_pin = { data = { "AV3" } };

20

//////////////////////////////////
// USB
//////////////////////////////////

25
macro expr USBMaster_pin = { data = { "D17" } };

macro expr USBD_pins = { data = { "D15", "B13", "C14", "A12", "D14", "C13", "B12",
"D13" } };
```

macro expr USBMS_pins = { data = {"C16"} };

macro expr USBnRST_pins = { data = {"B15"} };

5

macro expr USBIRQ_pins = { data = {"D16"} };

macro expr USB_A0_pins = { data = {"A14"} };

10

macro expr USBnRD_pins = { data = {"B14"} };

macro expr USBnWR_pins = { data = {"C15"} };

macro expr USBnCS_pins = { data = {"A13"} };

15

#endif // _KOMPRESSOR_MASTER_HEADER

20

TOGETHER-012501-4322460